A picture containing room

Description automatically generated

SHARC BUOY HARDWARE RECOMENDATIONS

Author Jamie Jacobson  
Student Number: JCBJAM007  
Date: 22 June 202

### This Document outlines required changes to the current PCBs to make the system compatible with the STM32L4

Table of Contents

1. [Introduction 1](#_Toc46312071)

[1.1. Reserved Pins 3](#_Toc46312072)

[1.1.1 Clock Pins 3](#_Toc46312073)

[Summary: 3](#_Toc46312074)

[1.1.2 Wake Up Pins 3](#_Toc46312075)

[Summary: 3](#_Toc46312076)

[2.1. Summary 4](#_Toc46312077)

[2.2. Debug Pins. 5](#_Toc46312078)

[2.3. GPS 6](#_Toc46312079)

[2.4. Flash Chips. 6](#_Toc46312080)

[2.5. Iridium 7](#_Toc46312081)

[Recommendations: 7](#_Toc46312082)

[2.6. BMP280 8](#_Toc46312083)

[2.7. INA219 Current Sensor 8](#_Toc46312084)

[2.8. MPU6050 8](#_Toc46312085)

1. Introduction

The Following document outlines hardware changes required to allow the STM32L476RG microcontroller to interface with the SHARCBUOY system. Version 2.0 was designed for the STM32F446RE microcontroller which has some similarities to the L4 however, fundamental pin changes. In addition, some sensors have not been optimally integrated into the SHARCBUOY system. This may be due to omitted pin traces as well as incorrect pin mapping. It may be required that an interrupt pin is required and must be mapped to an onboard wake up pin. Therefore, this document aims to assist with hardware changes as well as to provide a full Pin/memory map for the new System

# Reserved Pins

Some Pins on the stm32l4 microcontroller cannot be used for external mapping. These pins have a specific function and must be received for special cases. In addition, Certain clock/ calibration configurations require that these pins be reserved for clock inputs

## Clock Pins

Version 2.1 of the SHARC Buoy uses the MSI PLL as a source for the system clock. This configuration uses an external 32.768 KHz oscillator as a reference[[1]](#footnote-1). In order to achieve this, Pins PC14 and PC15 are reserved as OSC32\_OUT and OSC32\_IN respectively. This also allows the device to use the LSE oscillator as a clock source for the RTC.

### Summary:

|  |  |  |  |
| --- | --- | --- | --- |
| **Pin Name** | **Function** | **GPIO PORT** | **GPIO Pin** |
| OSC32\_IN | LSE 32.768 KHz input | GPIOC | PC14 |
| OSC32\_OUT | LSE 32.768 KHz GND ref | GPIOC | PC15 |

## Wake Up Pins

The STM32l4 Microcontroller has 5 Wake Up pins. These are GPIO Pins that can be configured to wake up the device from any low power mode. These pins are fundamental to allow the buoy to receive messages from the satellite at any point in its operation as well as to allow the IMU to detect events in sleep mode. Therefore, it is unadvisable to connect these pins to any external pin other than an interrupt pin otherwise, the wake-up pins get blocked and functionality is reduced. In addition, incorrect pin mapping and pin configuration can result in sporadic wake ups and unpredictable behavior which can cause the buoy to desynchronies from the primary loop. The Wake-up pins are listed in the table below.

### Summary:

|  |  |  |
| --- | --- | --- |
| **Pin Name** | **GPIO Port** | **GPIO Pin** |
| Wake Up Pin 1 | GPIOA | PA0 |
| Wake Up Pin 2 | GPIOC | PC13 |
| Wake Up Pin 3 | GPIOE | PE6 |
| Wake Up Pin 4 | GPIOA | PA2 |
| Wake Up Pin 5 | GPIOC | PC5 |

1. SHARC BUOY Pin Requirements

# Summary

A picture containing screenshot

Description automatically generated

Figure 1: STM32L476 Pinout showing allocated pins

|  |  |
| --- | --- |
| Key: |  |
|  | GPIO I/O Pin |
|  | USART Pin |
|  | I2C Pin |
|  | SPI Pin |

|  |  |
| --- | --- |
|  | Power Supply |
|  | Ground |
|  | Reserved |

|  |  |  |  |
| --- | --- | --- | --- |
| **DIGITAL IO** | | | |
| **GPIO Type** | **GPIO Port** | **GPIO Pin** | **PIN Function** |
| Output | PORTA | PA10 | BMP280 CS Pin |
| Input | PORTA | PA11 | IRIDIUM NETWORK AVAILABLE |
| Output | PORTA | PA4 | FLASH CHIP 4 CS |
| Output | PORTA | PA5 | NUCLEOL4 LED |
| Output | PORTB | PB0 | FLASH CHIP 3 CS |
| Output | PORTC | PC0 | FLASH CHIP 1 CS |
| Output | PORTC | PC1 | FLASH CHIP 2 CS |
| Input | PORTC | PC13 | IRIDIUM Ring Indicator |
| Output | PORTC | PC3 | FLASH CHIP WP |
| Input | PORTC | PC5 | MPU6050 INT Pin |
| Output | PORTC | PC7 | IRIDIUM On\_Off Pin |
| **UART** | | | |
| **UART Port** | **Rx Pin** | **Tx Pin** | **UART Description** |
| USART2 | PA2 | PA3 | Debug USART |
| UART4 | PC11 | PC10 | GPS USART |
| UART5 | PD2 | PC12 | IRIDIUM USART |
| **I2C** | | | |
| **I2C Port** | **SCL Pin** | **SDA Pin** | **I2C Description** |
| I2C2 | PB10 | PB11 | INA219 I2C |
| I2C1 | PB8 | PB9 | MPU6050 I2c |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **SPI** | | | | |
| **SPI Port** | **SCK Pin** | **MISO Pin** | **MOSI Pin** | **SPI Description** |
| SPI2 | PB13 | PB14 | PB15 | FLASH CHIP SPI |
| SPI1 | PB3 | PB4 | PB5 | BMP280 SPI |

## Debug Pins.

Debug allows the microcontroller to interface with the nucleo-l4 onboard LED and output data to a terminal via USART over USB. This allows the user to debug more easily and follow the program.

The proposed pin map for these peripherals are:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
|  | **STM32L476RG Function** | **Port** | **External Pin Name** | **AF Mapping** |
|  | GPIO Output | PA5 | LED 2 Pin | - |
|  | USART2\_Tx | PA2 | Serial Tx Pin | AF7 |
|  | USART2\_Rx | PA3 | Serial Rx Pin | AF7 |
|  | *GPIO Input* | PC13 | Push Button 1 | - |

# GPS

The Sharc buoy system uses a UBLOX neo GPS. The current version (NEO 6/7 m) IS a 3.3V USART chip with an additional PPS output. The following is a proposed pin mapping for the GPS module

|  |  |  |  |
| --- | --- | --- | --- |
| **STM32L476RG Function** | **Port** | **External Pin Name** | **AF Mapping** |
| UART4\_Tx | PC10 | GPS Rx Pin | AF8 |
| UART4\_Rx | PC11 | GPS Tx Pin | AF8 |
| TIM2\_CHANNEL2 | PA1 | GPS Input Capture | AF1 |
| Wake UP Pin 3\* | PE6 | GPS Interrupt Pin | - |

\*Note: The new neo 9m module contains additional pins which can be very beneficial for extended operations. The inclusion of an Interrupt pin will allow for asynchronous/ passive gps signal acquisition which can improve the lifespan of the device. A recommendation is to map this pin to wake up pin 3 (PE6).

## Flash Chips.

The device utilizes the AT45DB641E-SHN-T 64 M-Bit SPI Flash chips for permanent storage of data. The current hardware config allows for 4 chips to be connected in parallel to a singular SPI port. The pinout configuration for the chips are as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| GPIO Output | PC0 | Chip 1 Select | - |
| GPIO Output | PC1 | Chip 2 Select | - |
| GPIO Output | PB0 | Chip 3 Select | - |
| GPIO Output | PA4 | Chip 4 Select | - |
| GPIO Output | PC3 | Write Protect | - |
| SPI2\_CK | PB13 | SPI CLOCK | AF5 |
| SPI2\_MISO | PB14 | SP MISO Pin | AF5 |
| SP2\_MOSI | PB15 | SPI MOSI Pin | AF5 |

The previous pin mapping for the STM32F4 maps to the STM3L4 in a similar manner and does not require any other hardware alterations.

## Iridium

The device uses a satellite modem to transmit data from a remote location via the Iridium Satellite Constellation. A Rock block 9603 modem is used to communicate with the network and can transmit a maximum of 340 bytes in a single transmission session. The microcontroller can interface with the modem by sending AT commands over USART at a fixed baud rate of 19200 bit/s. The system has additional RTS and CTS pins for RS232 flow control however, the default communication setting does not require this and therefore is left out. The modem also contains 2 Indicator output pins: NetAv – active high when enough network signal is available to transmit a message, Ring Indicator – Alerts device when an incoming Satellite message is available. Finally, the device has a control pin that turns the modem on and off. This significantly reduces the power output and keeps the modem in a low power state.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **BUOY HEADER PIN** | **MODULE/CHIP PINS (IF USED)** | **MODULE/CHIP PIN NAME** | **STM32 BOARD NET NAME** | **STM32F446RE MAPPING** | **F446RE PORT** | **TYPE** |
| **1** | 8 | 5v in | +5V |  |  | POWER |
| **2** | 6 | TXD | IRID\_TX | UART5\_TX | PC12 | UART TX |
| **3** | 4 | NetAv | IRID\_NETAV | GPIOC13 | PC13 | Digital Input |
| **4** | 5 | RI | IRID\_RI | GPIOC14 | PC14 | Digital Input |
| **5** | 1 | RXD | IRID\_RX | UART5\_RX | PD2 | UART RX |
| **6** | 7 | OnOff | IRID\_ONOFF | GPIOC15 | PC15 | Digital Output |
| **7** | 10 | GND | GND |  |  | GROUND |

Note: The previous Iridium pin mapping for the STM32F4 is as follows.

This pin mapping results in several conflicts on the STM32l4 microcontroller. The pins RI (PC14) and OnOff (PC15) are reserved for the LSE oscillator input and output. The Pin NetAv is mapped to a wake-up pin which should rather be mapped to the Ring Indicator Pin. This will allow for the device to asynchronously receive satellite messages even while in sleep mode. Therefore, the following pin map is suggested for the STM32l4

|  |  |  |  |
| --- | --- | --- | --- |
| GPIO Output | PC7 | On Off Pin | - |
| GPIO Input | PC13 | Ring Indicator | - |
| GPIO Input | PA11 | Network Available | - |
| UART5\_Tx | PC12 | Serial Tx Pin | AF8 |
| UART5\_Rx | PD2 | Serial Rx Pin | AF8 |

### Recommendations:

In the future, additional hardware recommendations are:

1. Move Ring Indicator to PC13 (Wake Up Pin 2)
2. Move UART5 Rx, Tx Pins to LPUART (PC0, PC1)

# BMP280

The BMP 280 is an SPI/I2C digital environmental sensor for sampling pressure and temperature. The system interfaces with the device via SPI on SPI1. The device has no other interrupt pins and a single digital input for chip select. The Pin Mapping remains largely unchanged as there are no conflicts on the stm32l4. The Pin map is as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| GPIO Output | PA10 | Chip Select Pin | - |
| SPI1\_CK | PB3 | SPI CLOCK | AF6 |
| SPI1\_MISO | PB4 | SPI MISO | AF6 |
| SPI1\_MOSI | PB5 | SPI MOSI | AF6 |

# INA219 Current Sensor

The device uses the INA219 I2C current sensor to measure Shunt Voltage, Battery Voltage, Current and power. The device will be used to monitor the onboard battery to ensure the device draws a steady current. The microcontroller interfaces with the device through I2C2 which, on the stm32l4 is on different pins to the stm32F4. On the STM32L4, I2C2 is on Pins PB10 (I2C2\_SCL) and PB11 (I2C\_SDA) (I2C\_SDA). The New pinout is shown in the table below

|  |  |  |  |
| --- | --- | --- | --- |
| I2C2\_SCL | PB10 | I2C Serial Clock Line | AF4 |
| I2C2\_SDA | PB11 | I2C Serial Data Line | AF4 |

# MPU6050

The MPu6050 is a 6 DOF I2C IMU. The device contains an accelerometer and a gyro. In addition, the device has an onboard Digital Low Pass filter and digital motion processor. The I2C Pin mapping remains largely unchanged however, previous version of the hardware did not accommodate for the device’s interrupt pin. This can cause synchronization issues as well as a loss of functionality. It is recommended to incorporate an interrupt pin into the hardware in order to allow for interrupt-based sampling as well as asynchronous event detection. This can be achieved by mapping the interrupt pin to Wake Up Pin 5 (PC5).

Hence, The New PCB Pin Map is shown in the table below

|  |  |  |  |
| --- | --- | --- | --- |
| I2C1\_SCL | PB8 | I2C Serial Clock Line | AF4 |
| I2C1\_SDA | PB9 | I2c Serial Data Line | AF4 |
| GPIO Input | PC5 | Interrupt Pin | - |

1. Conclusion

These hardware changes should result in a more optimal system with increased functionality and power saving performance. In addition, more asynchronous behavior is introduced allowing for faster, more autonomous operability.

1. See Document: Power Mode and Clock Selection for more information [↑](#footnote-ref-1)